Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **INV. INPUT**
2. **NONINV. INPUT**
3. **SYNC**
4. **OSC OUTPUT**
5. **CT**
6. **RT**
7. **DISCHARGE**
8. **SOFT-START**
9. **COMPENSATION**
10. **SHUTDOWN**
11. **OUTPUT A**
12. **GROUND**
13. **VC**
14. **OUTPUT B**
15. **VCC**
16. **VREF**

**EA**

**1525A**

**12**

**13**

**14 11**

**15**

**16**

**1**

**2**

**3 4 5 6**

**10**

**9**

**8**

**7**

**MASK**

**REF**

**.088”**

**.095”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: 1525A**

**APPROVED BY: DK DIE SIZE .088” X .095” DATE: 8/25/21**

**MFG: SILCON GENERAL THICKNESS .015” P/N: SG3525A**

**DG 10.1.2**

#### Rev B, 7/1